REMARKS

Objection to the Drawings

The examiner objected to the drawings for purportedly not showing the passivation layer covering the flash memory cell. Figure 1 shows passivation layer 103 covering semiconductor substrate 101. The specification states that semiconductor substrate 101 "includes conventional flash memory features, including flash memory cells (not shown)." (See specification at page 3, lines 20-22.) Because the drawings show passivation layer 103 covering substrate 101, which includes flash memory cells, it necessarily follows that the drawings show passivation layer 103 covering the flash memory cells.

The drawings do not need to provide additional detail for the flash memory cells located in substrate 101. Because flash memory cells are conventional features of a flash memory, it is appropriate to illustrate them schematically. In this regard, 37 C.F.R. §1.83(a) provides:

> . . . conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a labeled rectangular box).

Flash memories necessarily have flash memory cells. Figure 1 illustrates this feature schematically as it is a conventional feature for which a detailed illustration is not essential for a proper understanding of the invention. As the specification describes, and as figure 1 illustrates, the invention pertains to forming a passivation layer from a material that is opaque to ultraviolet light, which covers conventional flash memory cells that all flash memories contain.

There is no reason to include in the drawings unnecessary detail that relates to such a conventional component.

Because applicants' figure 1 schematically represents a conventional flash memory structure, which necessarily includes flash memory cells, in precisely the manner 37 C.F.R. §1.83(a) recommends, there is no reason to modify the drawing to include additional detail. For that reason, applicants respectfully request the examiner to withdraw the objection to the drawings.

Rejection Under 35 U.S.C. §112

The examiner rejected claims 9-15 under 35 U.S.C. §112, first paragraph, for purportedly containing subject matter that was not described in the specification. Specifically, the examiner contends that the phrase "the passivation layer covering the flash memory cell" is not supported by the original specification. Applicants disagree.

The subject matter of a later claim need not be described literally (or "*in haec verba*") for the specification to satisfy the description requirement. "Instead, the disclosure need only reasonably convey to persons skilled in the art that the inventor had possession of the subject matter in question." Fujikawa v. Wattanasin, 93 F.3d 1559, 1570 (Fed. Cir. 1996); see also Union Oil Co. of California v. Atlantic Richfield Co., 208 F.3d 989, 997 (Fed. Cir. 2000), cert. denied, 121 S. Ct 1167 (2001); Purdue Pharma L.P. v. Faulding Inc., 230 F.3d 1320, 1323 (Fed. Cir. 2000); and Lampi Corp. v. American Power Products, Inc., 228 F.3d 1365, 1378 (Fed. Cir. 2000).

If a person of ordinary skill in the art would have understood the inventor to have been in possession of the claimed invention at the time of filing, even if every nuance of the claims is not explicitly described in the specification, then the adequate written description requirement is met. In re Alton, 76 F.3d 1168, 1175 (Fed. Cir. 1996).

As already indicated, figure 1 shows passivation layer 103 covering semiconductor substrate 101. The specification states that semiconductor substrate 101 "includes conventional flash memory features, including flash memory cells (not shown)." (See specification at page 3, lines 20-22.) Because passivation layer 103 covers substrate 101, which includes flash memory cells, it necessarily follows that passivation layer 103 covers the flash memory cells.

The specification (at page 6, line 3, through page 7, line 2) confirms that passivation layer 103 covers the flash memory cells that are included in the claimed flash memory. Here, the specification describes forming an ultraviolet ("UV") opaque passivation layer, which comprises a silicon nitride barrier layer 104 and a polyimide stress reduction layer 105. The silicon nitride layer is formed using a conventional plasma enhanced chemical vapor deposition ("PECVD") process, and the polyimide layer is spun onto the silicon nitride layer. Because such PECVD and spin-on processes deposit these materials over the entire structure, the resulting passivation layer must necessarily cover the device's flash memory cells. Although part of passivation layer 103 is subsequently removed to form bond pads, those skilled in the art would appreciate that this step will not expose the underlying flash memory cells.

For these reasons alone, anyone skilled in the art will immediately recognize that the structure applicants described in the original specification includes a passivation layer that covers the claimed device's flash memory cells. This is even more evident given that the benefit applicants' new process provides is that it permits a UV opaque passivation layer to cover the flash memory cells of a flash memory.

As explained in the Background of the Invention section of the specification, charge may build up on the floating gates of the flash memory cells as the device is made. The device is exposed to UV radiation to neutralize that charge. Prior to applicants' invention, that exposure step was applied after the passivation layer was formed. As a result, previous flash memories could not include a UV opaque passivation layer because such a layer would prevent UV radiation from reaching the flash memory cells' floating gates. A UV opaque passivation layer would prevent UV radiation from reaching the flash memory cells because the passivation layer covered them.

To enable a flash memory to include a UV opaque passivation layer, applicants devised the process claimed in U.S. Patent No. 6,350,651. That patent issued from the parent application from which the pending divisional application claims priority. That process exposes the device to UV light to neutralize process induced charge before forming the passivation layer. This change in process sequence enables a UV opaque passivation layer to be formed – notwithstanding the fact that the passivation layer must cover the flash memory cells. The examiner must recognize that there would not be any

advantage to applicants' new process, over prior practice, unless the passivation layer in the claimed flash memory covered the flash memory cells.

Because the passivation layer in a flash memory device covers the flash memory cells, prior processes required a UV transparent passivation layer to enable UV light to reach the flash memory cells. Applicants' patented process enables a UV opaque passivation layer to be used instead, despite the fact that it covers the flash memory cells, because applicants' process exposes the device to UV light (to neutralize process induced charge) before forming the passivation layer. Anyone skilled in the art would thus appreciate, based on the basic structure of flash memories and the nature of applicants' invention, that applicants' specification must disclose a flash memory with a passivation layer that covers the flash memory cells.

For the reasons set forth above, applicants' specification supports the phrase "the passivation layer covering the flash memory cell," despite not including these precise words. In this regard, applicants invite the examiner to consider In re Wright, 866 F.2d 422 (Fed. Cir. 1989). In that case, the Court of Appeals for the Federal Circuit reversed a decision from the Board of Patent Appeals and Interferences, which had upheld the rejection of an amended claim under 35 U.S.C. §112, first paragraph, based on the specification supposedly not providing an adequate written description of a particular element.

In In re Wright, the rejected claim covered a method of forming images that included depositing a layer of photosensitive microcapsules in the form of a free-flowing powder. The claim had been amended by adding a limitation, which

specified that the powder be "distributed upon said support but not perman ntly fixed thereto." The specification, as filed, did not include the exact phrase "not permanently fixed." Nonetheless, the Court held that the original disclosure unequivocally taught the absence of permanently fixed microcapsules. The Court supported that conclusion by noting that the specification's examples indicated that the microcapsules should be distributed so as not to change their position until the image is formed by rupturing. Because those examples suggested that the microcapsules' position would be changed after the image was formed, they demonstrated that the microcapsules were not permanently fixed – as specified in the amended claim.

As in In re Wright, applicants' drawings and specification indicate that the passivation layer must cover the flash memory cells – even though the specification does not provide the precise language that was added to amended claim 9. That disclosure, when considered with the nature of applicants' invention (i.e., applying the UV exposure step prior to forming the passivation layer to enable a UV opaque passivation layer to cover the flash memory cells) and the basic fact that the typical flash memory structure fundamentally includes a passivation layer that covers the flash memory cells, establishes that applicants' disclosure supports the phrase "the passivation layer covering the flash memory cell." Accordingly, applicants respectfully request the examiner to withdraw the rejection of claims 9-15 under 35 U.S.C. §112.

Rejection Under 35 U.S.C. §102(b)

The examiner rejected claims 9-11 and 15 under 35 U.S.C. §102(b) as being anticipated by Kiyohiko. To support that rejection, the examiner contends that Kiyohiko describes a flash memory with the passivation layer covering the flash memory cell. Specifically, the examiner contends that an EPROM is a type of flash memory, that "passivation layer 9" covers the flash memory cell, and that "passivation layer 10" covers at least a portion of the flash memory cell.

Claims 9-11 and 15 define a flash memory. Kiyohiko does not describe a flash memory. Kiyohiko instead describes an EPROM that is erased by exposing it to UV radiation. In contrast, a flash memory (e.g., a flash EPROM) is a type of programmable read only memory that is erased electrically. Kiyohiko's UV erasable EPROM is not a type of flash memory, as the examiner suggests. The examiner's reliance on page 2, lines 12-16, of applicants' specification is misplaced. That excerpt simply mentions that flash memories are erasable programmable read only memories that may be erased electrically. It does not suggest that a UV erasable EPROM, like the one Kiyohiko describes, is a flash memory. Because Kiyohiko describes a UV erasable EPROM – not a flash memory, that reference does not anticipate claims 9-11 and 15.

Kiyohiko does not anticipate those claims for another reason. Claim 9 requires the UV opaque passivation layer to cover the flash memory cell. Because flash memories do not require UV exposure to erase them, they may remain operable even when their flash memory cells are covered with such a passivation layer. As explained above, applicants' patented process permits a

flash memory to include a UV opaque passivation layer, because that process – unlike previous processes -- applies the required UV exposure step before forming the passivation layer.

In contrast to applicants' claimed flash memory, Kiyohiko's UV erasable EPROM must permit UV radiation to reach its memory cells. For that reason, Kiyohiko's device must include a window within the passivation layer (e.g., its window 11 that is formed within polyimide film 10) to enable UV radiation to reach its memory cells. Because Kiyohiko's EPROM does not (and cannot) include a passivation layer that covers its memory cells, Kiyohiko's device does not anticipate the flash memory of applicants' claims 9-11 and 15 for this additional reason.

The examiner's suggestion that Kiyohiko's silicon nitride film 9 and polyimide film 10 are each passivation layers is baseless. Anyone skilled in the art will realize that Kiyohiko's passivation layer includes both the silicon nitride film and the polyimide film. Likewise, the examiner's contention that Kiyohiko's passivation layer covers the "flash memory cells" is without merit. Because Kiyohiko's device is not a flash memory, it lacks flash memory cells that a passivation layer may cover.

More importantly, as already noted, Kiyohiko's UV erasable EPROM cannot function if a UV opaque passivation layer covers it's memory cells. To erase Kiyohiko's EPROM, UV light must reach the device's memory cells. That is why Kiyohiko must remove the passivation layer where it covers the memory cells. When relying on Kiyohiko's suggestion that "It is not necessary to provide

the window 11 to each EPROM element," the examiner neglects the remainder of the sentence, which states: "one [i.e., a window] can be provided to an entire of the [sic] EPROM part." Read in context, that sentence simply offers an alternative to including a discrete window for each EPROM element to enable UV light to access each element – namely, to instead incorporate into the part a window that exposes the entire EPROM part. That sentence does not suggest that Kiyohiko's device may include a passivation layer that covers one or more memory cells. On the contrary, it simply suggests that either discrete or blanket removal of the passivation layer may be applied to expose the memory cells.

The claimed invention relates to flash memories, not UV erasable EPROMs. In addition, the claimed invention requires the passivation layer to cover the flash memory cell – a feature that Kiyohiko's EPROM lacks. For these reasons, Kiyohiko does not anticipate the flash memory of amended claim 9. Because claims 10, 11 and 15 depend upon amended claim 9, Kiyohiko does not anticipate those claims either. Accordingly, applicants respectfully request the examiner to withdraw the rejection of these claims based upon Kiyohiko allegedly anticipating them.

Rejection Under 35 U.S.C. §103(a)

The examiner rejected claims 12-14 under 35 U.S.C. §103(a) as being unpatentable over Kiyohiko in view of Jeuch. These claims depend upon amended claim 9. As explained above, amended claim 9 requires the UV opaque passivation layer to cover the flash memory cell. Neither Kiyohiko nor Jeuch describes a flash memory that includes this feature. Nor does either

reference provide any teaching or suggestion that would have motivated one skilled in the art to modify any of the devices they describe by incorporating into them a UV opaque passivation layer that covers a flash memory cell.

On the contrary, Kiyohiko teaches away from including such a feature in such a device. Kiyohiko teaches to form a window through the passivation layer to enable UV radiation to reach the memory cells. Because Kiyohiko's EPROM can be erased only by exposing the memory cells to UV radiation, modifying that device to cause a UV opaque passivation layer to cover the memory cells would have rendered it inoperable. Because those skilled in the art would have recognized that covering the memory cells in Kiyohiko's EPROM with a UV opaque passivation layer would yield an inoperative device, it would not have been obvious to them to modify that device in that way.

Unlike Kiyohiko's EPROM, flash memories do not require UV exposure to erase them. For that reason, they may be erased even when their flash memory cells are covered with a UV opaque passivation layer. Notwithstanding that fact, conventional wisdom – prior to applicants' invention – held that even flash memories could not include a UV opaque passivation layer that covers the flash memory cells. The reason why is because even these devices' memory cells required UV exposure to neutralize any electronic charge that had built up on the memory cells during the process for making the device. Because that UV exposure step was performed after the passivation layer was formed, it was not possible for the device to include a UV opaque passivation layer that covered the flash memory cells.

Applicants discovered that such a UV exposure step could effectively neutralize electric charge -- even when applied before forming the passivation layer, as long as that UV exposure step was performed after patterning the final metal layer. Not until applicants invented that now patented process was it even possible to make the flash memory of amended claim 9, which includes a UV opaque passivation layer that covers the flash memory cell. It logically follows that the claimed flash memory is patentable for essentially the same reasons that the process for making it is patentable – as the Patent Office previously acknowledged when issuing U.S. Patent No. 6,350,651.

For the reasons set forth above, the flash memory of amended claim 9 is patentable over the combination of Kiyohiko and Jeuch. Because claims 12-14 depend upon amended claim 9, they are likewise patentable over the cited prior art. Consequently, applicants request the examiner to withdraw the rejection of these claims based on 35 U.S.C. §103(a).

The flash memories claimed in all pending claims are patentable over the cited references, either when considered alone or in combination. Accordingly, applicants respectfully request the examiner to allow pending claims 9-15, as amended, to issue.

Respectfully submitted,

Date: January 28, 2003

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VERSION OF SPECIFICATION EXCERPT WITH MARKINGS TO SHOW CHANGES MADE

Amended paragraph beginning at page 2, first line:

This is a Divisional Application of Serial No.: 09/330,257 filed June 10, 1999, [which is presently pending] now U.S. Patent No. 6,350,651.

CERTIFICATE OF TRANSMISSION
(37 C.F.R. § 1.8(a))

I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office on January 28, 2003.

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